

What is claimed is:

- 1 Claim 1. A method and apparatus for real time capture of the desired failing chip memory cell diagnostic information from high speed testing of a semiconductor chip, comprising the steps of:

collecting data from scanning the circuits of said semiconductor chip for a failing cell for immediate scan-out off-chip at a level of assembly test, said level of assembly test being selected from a group consisting of: an initial manufacturing wafer test, a module test, a system level test, regardless of the clocking methodology, and

providing not only for the data collection of the first failing cell, and then skipping the collection of data up to a programmed amount to skip up to an "N<sup>th</sup>" failing cell and recording the failure of the subsequent "N<sup>th</sup>" + 1 fail.

2. The method according to claim 1 wherein the semiconductor chip is provided with supplemental address registers which supplement existing address registers for providing data synchronous with fail determination circuits, employing ABIST comparison circuit to obtain a bit wise fail result vector corresponding to each device data out of a device under test, and wherein said bit wise fail result vector feeds a detect and encode circuit that determines if one and only one device data out failed, and if so, provides an encoded "address" that is concatenated to a corresponding register address field.

3. The method according to claim 2 wherein said result vector is fed thereafter into a hold and compare function circuit having a hold portion of the function providing for the "full" fail address field comprising the memory address of the device under test plus the failing output encoded address for identifying the failing location to be stored in

a LSSD register of said semiconductor chip, and wherein the compare function provides for identification recording of subsequent unique and different failing locations to be identified in the device under test.

4. The method according to claim 3 wherein said hold and compare function circuit is configured to load the first and reload each subsequent unique failing location encountered, decrementing a programmable skip counter at each unique fail encountered, until the skip counter reaches a final "zero" state.

5. The method according to claim 4 wherein said hold and compare function circuit is configured to load the first and reload each subsequent unique failing location encountered, decrementing a programmable skip counter at each unique fail encountered, until the skip counter reaches an intended " $N^{\text{th}}$ " fail to be recorded.

6. The method according to claim 5 wherein said hold and compare function circuit allows said programmable skip counter to record a zero state as a default thus enabling the first fail to be recorded.

7. The method according to claim 1 wherein said supplemental address registers include a fail trap register, and there is provided a programmable skip fail counter, and a hold and compare function circuit, and wherein said programmable skip counter is enabled for initialization to a "record first fail" mode, and then with non-zero values of the skip counter to a "record  $N^{\text{th}}+1$  fail" mode, wherein said "Record first fail" is considered the default or base function when the initial state of all registers is defined to be "0", and

is obtained through scan initialization of the LSSD registers of the semiconductor chip.

POU9-2001-0050-US1